

Form 1449*	Atty. Docket No.: 303.678US4	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Kie Y. Ahn et al.	
	Filing Date: Herewith	Group: ²⁸⁷⁸ Unknown

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
<u>PD</u>	5,668,035	09/16/1997	Fang, C.H., et al.	438	239	06/10/96
<u>PD</u>	5,985,725	11/16/1999	Chou, J.	438	294	12/23/97
<u>PD</u>	6,087,225	07/11/2000	Bronner, G.B., et al.	438	275	02/05/98
<u>PD</u>	6,097,056	08/01/2000	Hsu, L.L., et al.	257	315	04/28/98
<u>PD</u>	6,222,788	04/01/2001	Forbes, et al.	365	230.06	

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
-----------------------	-----------------	------	---------	-------	----------	-------------------------

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
<u>PD</u>	Chen, Y., et al., "Performance and Reliability Assessment of Dual-Gate CMOS Devices with Gate Oxide Grown Nitrogen Implanted Si Substrates", <u>International Electron Device Meeting</u> , pg. 1-4, (1997)
<u>PD</u>	Cho, I.H., et al., "Highly Reliable Dual Gate Oxide Fabrication by Reducing Wet Etching Time and Re-Oxidation for Sub-Quarter Micron CMOS Devices", <u>Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials</u> , pgs. 174-175, (1999)
<u>PD</u>	Crowder, S., et al., "Trade-offs in the Integration of High Performance Devices with Trench Capacitor DRAM", <u>Dig. Int. Electron Devices Meeting, Washington, D.C.</u> , pp. 45-48, (Dec. 1997)
<u>PD</u>	Fujiwara, M., et al., "New Optimization Guidelines for Sub-0.1 micrometer CMOS Technologies with 2 micrometer
<u>PD</u>	Guo, X., et al., "High Quality Ultra-thin TiO ₂ /Si ₃ N ₄ Gate Dielectric for Giga Scale MOS Technology", <u>Technical Digest of 1998 IEDM</u> , pp. 377-380, (1998)
<u>PD</u>	Han, L.K., et al., "Electrical Characteristics and Reliability of sub-3 nm Gate Oxides Grown on Nitrides Implanted Silicon Substrates", <u>Int. Electron Devices Meeting, Washington, D.C.</u> , pp. 1-4, (1997)

Examiner PHUO T. DANG Date Considered 8/25/2000

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial of citation considered, whether or not citation is in conformance with MPEP 2109; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

11046 U.S. PTO
09/941393
08/30/01

Form 1449*	Atty. Docket No.: 303.678US4	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Kie Y. Ahn et al.	
	Filing Date: Herewith	Group: ²⁸¹⁹ Unknown

OTHER DOCUMENTS

**Examiner
Initial

(including Author, Title, Date, Pertinent Pages, Etc.)

PD	Hideo, O., et al., "Dual Gate Oxide Process Integration for High Performance Embedded Memory Products", <u>Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials</u> , pp. 108-109, (1998)
PD	King, Y., et al., "Sub-5nm Multiple-Thickness Gate Oxide Technology Using Oxygen Implantation", <u>IEDM Technical Digest</u> , pp. 585-588, (1998)
PD	Liu, C.T., et al., "Multiple Gate Oxide Thickness for 2GHz System-on-A-Chip Technologies", <u>IEDM Technical Digest</u> , pp. 589-592, (1998)
	Ma, T.P., "Making Silicon Nitride film a Viable Gate Dielectric", <u>IEEE Trans. On Electron Devices</u> , 45(3), pp. 680-690, (1998)
PD	Muller, D.A., et al., "The Electronic Structure at the Atomic Scale of Ultrathin Gate Oxides", <u>Nature</u> , 399, 758-761, (June 1999)
PD	Oi, H., et al., "Dual Gate Oxide Process Integration for High Performance Embedded Memory Products", <u>Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials</u> , pp. 108-109, (1998)
PD	Saito, Y., et al., "High-Integrity Silicon Oxide Grown at Low-temperature by Atomic Oxygen Generated in High-Density Krypton Plasma", <u>Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials</u> , pp. 152-153, (1999)
PD	Togo, M., et al., "Multiple-Thickness Gate Oxide and Dual-Gate Technologies for High Performance Logic-Embedded DRAMs", <u>IEDM Technical Digest</u> , pp. 347-350, (1998)
PD	Tseng, H., et al., "Application of JVD Nitride Gate Dielectric to A 0.35 Micron CMOS Process for Reduction of Gate Leakage Current And Boron Penetration", <u>Int. Electron Device Meeting</u> , San Francisco, CA, pp. 1-4, (1998)

Examiner

PHU T DANG

Date Considered

4/24/2003

PD

*Supplemental Disclosure Statement Form (FD-1449)

**EXAMINER: Initial if citation considered, whether or not cited. If in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.